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Family of Multiport Switched-Capacitor Multilevel Inverters for High Frequency AC Power Distribution

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***Abstract*—This paper proposes a family of multiport switched-capacitor multilevel inverter (SCMLI) topologies for high frequency AC power distribution. It employs asymmetric DC voltage sources with a common ground which makes it ideal to be employed in renewable energy farms and modern electric vehicles. The proposed family of step-up SCMLI attains higher number of output voltage steps with optimum component count in comparison to several existing topologies. The problem of capacitor voltage balancing is solved as the capacitors are inherently charged to a finite voltage every half cycle. In-depth study on two staircase modulation strategies, namely selective harmonic elimination and minimum total harmonic distortion scheme is presented with study on the variation of switching angles and THD with modulation indices under both schemes. Working principle and analysis are presented for the proposed family of topologies. Simulation outcomes are validated with experimental results under both the aforementioned modulation schemes with equal and unequal output voltage waveform steps.**

***Index Terms*—H-bridge, HFAC power distribution, high frequency DC/AC Inverter, multilevel inverter, selective harmonic elimination, pulse width modulation, switched-capacitor, total harmonic distortion**

I. Introduction

HIGH Frequency Alternating Current Power Distribution Systems (HFAC PDS) offer numerous benefits over conventional DC PDS. Principle advantage is that HFAC PDS omits the rectifier and a filter stage in front end, and an inverter stage in the point of load power supply [1]. The reduction in the number of power processing stages reflects as improved efficiency, fewer component count, higher reliability and lower cost. NASA, in 1980s, initiated research in HFAC PDS for their space station [2]. HFAC PDS have features that make them attractive to aerospace, telecommunication, lighting, computer power supply, micro-grids and automotive applications [1]–[8]. A HFAC PDS includes a HFAC source, a distribution track and point-of-load converters. This paper focuses on employing a switched-capacitor multilevel inverter (SCMLI) as an HFAC source.

Renewable energy farms have several DC sources, usually batteries. These inverters can effectively be utilized in such renewable energy based microgrids as it employs multiple DC input sources of different magnitude. HFAC PDS employing compact transformers, smaller filters and high density power converters offer several advantages to the micro-grids user [8]. HFAC distribution enables to filter out higher order harmonics relatively easily. Major hindrance for HFAC power distribution is the higher ohmic losses due to skin and proximity effects, and magnified impedance across the transmission line. Both these factors increase with increase in length of distribution and distribution frequency.

Multilevel inverters (MLI) have attained wide acceptance owing to the exciting features they offer. MLI output staircase waveforms which greatly mitigates the harmonic content when compared to traditional square wave inverters. MLI are generally classified into diode clamped, capacitor clamped (also referred to as flying capacitor) and cascaded multilevel inverters [9], [10]. Diode clamped MLI require many additional diodes as the level increases, the capacitor voltages are unbalanced and the voltage rating for the blocking diodes is high. Capacitor clamped MLI also suffer from voltage imbalance and require several additional storage capacitors as the voltage level increases which makes it more expensive and difficult during the package process. The major drawback in cascaded MLI is the necessity for separate isolated DC sources.

There has been growing interest in Switched-Capacitor Multilevel Inverters (SCMLI) over the past few years [11]–[26]. A seven-level SCMLI using series-parallel conversion employing a single DC source with comparison of level and phase-shifted PWM is presented in [11]. A generalized single-source step-up SCMLI capable of driving inductive loads is presented in [12]. A novel SCMLI proposed in [13] also utilizes a single DC source to obtain a voltage stepup. In [14], [15], an SC doubler circuit is employed with traditional cascaded H-bridge to obtain a relatively higher voltage step count with fewer components in comparison to the traditional cascaded MLI. The partial charging of SC technique discussed in [16] is relatively complicated as it is difficult to control the

This article is an extension of the conference paper titled "Switched-capacitor Multilevel Inverters for High Frequency AC Microgrids" presented at the 2017 Applied Power Electronics Conference and Exposition in Tampa, Florida, USA. S. Raghu Raman (raghu.sekhar@connect.polyu.hk), Yat Chi Fong (ycchi.fong@connect.polyu.hk) and corresponding author K.W.E Cheng (eeecheng@polyu.edu.hk) are with the Power Electronics Research Centre, Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong. Ye Yuanmao (yuanmao.ye@connect.polyu.hk) is with the School of Automation, Guangdong University of Technology, China.

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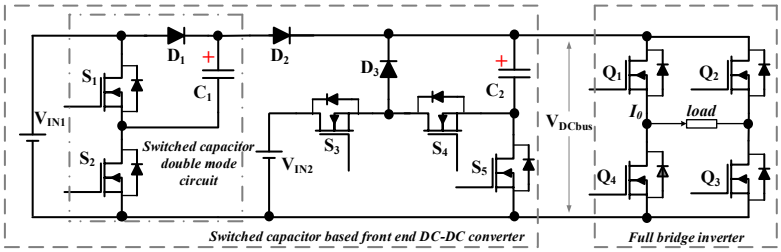
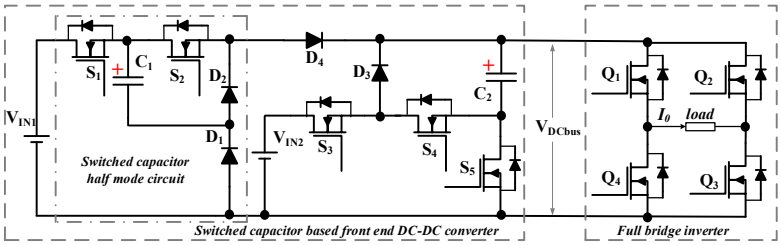


(a) Proposed topology A



(b) Proposed topology B

Fig. 1: Two basic proposed structures of SCMLI employing (a) SC voltage double mode circuit (b) SC voltage half mode circuit

charging profile of the boost SCMLI. In [17], a multi-source step-up SCMLI with reduced component count capable of driving inductive loads is presented. Similarly, in [18], multiple sources are utilized along with a single SC cell to realize a stepup SCMLI. A capacitive voltage divider technique is used to obtain a nine-level SCMLI in [19]. In [20], a novel SC cell with two capacitors in parallel with a DC source is proposed to realize a boost SCMLI capable of driving R-L loads. A hybrid nineteen-level MLI utilizing the features of both SC and flying capacitor technique is presented in [21]. In [22], the SCMLI utilizes the bipolar series-parallel or cross-switched SC technique to charge the switched-capacitors and to step-up the voltage. Asymmetric voltage sources are used to derive multilevel output voltage waveform without stepping up in [26].

SCMLI topologies in [11], [13], [19] employ a single voltage source to realize higher number of output voltage levels whereas [18], [23], [24], [26] employ multiple DC voltage sources. However, both these types operate by charging the parallel SC to input voltage and discharging it while connecting in series to the load. SCMLI are relatively more apt to high frequency output AC inverters [13] as the size of the energy storage capacitor at high frequency is small and the quality of output waveform is better with low distortion. Several switching techniques including phase shift [14], SHE [13], [24], level and phase shifted PWM [11] for SCMLI have been studied.

To realize a high frequency AC micro-grid of a few kWs, it is crucial to employ power converters with fewer components to realize a cost effective system with higher reliability. With the proliferation in renewable energy based solar and wind farms, such multi-input topologies gain tremendous potential. This would make it easier to convince the customers to participate; for example to install roof top solar panels with HFAC (or even LFAC) PV inverters. This new family of inverters naturally tend to use fewer components to realize a multilevel staircase output when compared to traditional topologies of MLI. Additionally, their operation principle charges the DC capacitor to a finite voltage each half cycle, which solves the voltage imbalance issue. However, there is a limitation on the power level these inverters can operate at. This limitation is due to the fact that the DC capacitor employed is used to feed the load during certain intervals of operation and there is an inherent limitation to it due to the voltage ripple. Also, at higher power levels, the size of the capacitor becomes larger. Higher capacitance also leads to spiky charging currents which can impact the life of a capacitor and lead to significant EMI issues.

II. Topologies for HFAC microgrids

Both the SCMLI topologies discussed in the following subsections are derived from [24]. The first topology (Fig.1a) increases the number of output voltage levels by employing an SC doubler circuit by cascading it with a voltage source. The second topology (Fig.1b) employing SC half circuit to increase the voltage levels. Both these basic nine-level topologies are generalized (Fig.4a and 4b).

A. Topology A description and operation principle

In the proposed SCMLI topology A shown in Fig. 1a, front end SC based DC-DC converter employs two input sources (V_{IN1} and V_{IN2}), five transistors (S_1, S_2, S_3, S_4 and S_5), three diodes (D_1, D_2 and D_3) and two capacitors (C_1 and C_2). DC levels obtained at the inverter DC bus include V_{IN1}, $2V_{IN1}$, V_{IN2}, $V_{IN1}+V_{IN2}$. The H-bridge inverter employing transistors Q_1 to Q_4 effectively outputs 8 bipolar levels ($\pm V_{IN1}$, $\pm 2V_{IN1}$, $\pm V_{IN2}$, $\pm(V_{IN1}+V_{IN2})$) and a zero across the load. For the purpose of primary analysis, it is assumed that the switches and the voltage sources employed are ideal;

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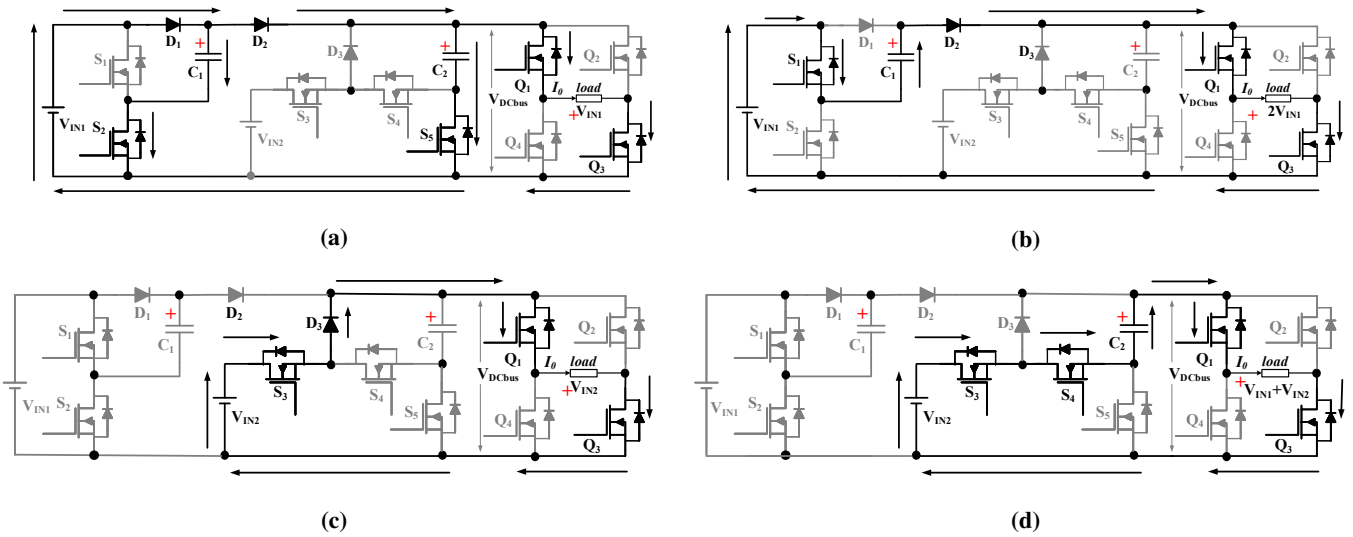

Fig. 2: Equivalent circuits of the proposed 9-level SCMLI to obtain different voltage levels (a) $V_o = V_{IN1}$ (b) $V_o = 2V_{IN1}$ (c) $V_o = V_{IN2}$ (d) $V_o = V_{IN1} + V_{IN2}$

capacitances (C_1 and C_2) are large enough to maintain a constant voltage and supply constant output current, and the voltage ripple across them is small enough to be neglected. Table 1 explains the switching logic of the proposed inverter. The working states are explained in the following subsections. In general, to obtain a positive voltage across the load, H-bridge transistors Q_1 and Q_3 are turned ON. Similarly, to obtain a negative voltage across the load, transistors Q_2 and Q_4 are turned ON.

TABLE I: Switching logic for the proposed topology A

S_1	S_2	S_3	S_4	S_5	V_{DCbus}
0	**1**	0	0	**1**	V_{IN1}
1	**0**	0	0	**0**	$2V_{IN1}$
0	**0**	1	0	**0**	V_{IN2}
0	**0**	1	1	**0**	V_{IN2}+V_{IN1}
0	**1**	0	0	**1**	0

TABLE II: Switching logic for proposed topology B

S_1	S_2	S_3	S_4	S_5	V_{DCbus}
1	0	0	0	1	$0.5V_{IN1}$
1	1	0	0	0	V_{IN1}
0	0	1	0	0	V_{IN2}
0	0	1	1	0	$0.5V_{IN1}$+V_{IN2}
0	1	0	0	1	0

1) Output voltage = $\pm V_{IN1}$ state: Capacitor C_1, is charged equal to the input voltage source V_{IN1} through D_1 by turning ON transistor S_2, while capacitor C_2 is charged to V_{IN1} by turning ON transistor S_5, through diodes D_1 and D_2. Transistors S_1, S_3, S_4 and diode D_3 remain turned OFF. The DC bus voltage at this state is equal to V_{IN1} as V_{IN2} is blocked by OFF transistor S_3. Fig. 2(a) depicts the equivalent state for $V_0 = +V_{IN1}$.

2) Output voltage = $\pm 2V_{IN1}$ state: Transistor S_1 is turned ON, while S_2 is OFF, which connects V_{IN1} in series with capacitor C_1 (charged to V_{IN1}) and diode D_2. At this state, V_{DCbus} is equal to $2V_{IN1}$. Transistors S_3, S_4 and S_5 remain turned OFF. Diodes D_1 and D_3 are reverse biased. Fig. 2(b) depicts the equivalent state for $V_0 = +2V_{IN1}$.

3) Output voltage = $\pm V_{IN2}$ state: For normal operation of the proposed inverter, $V_{IN2} > V_{IN1}$. In the SC front end DC-DC converter, only transistor S_3 is turned ON while other transistors are turned OFF. Therefore, V_{IN2} is connected to the DC bus through diode D_3. Diodes D_1 and D_2 are reverse biased and hence block V_{IN1}. Fig. 2(c) depicts the equivalent state for $V_0 = V_{IN2}$. During this interval, capacitor C_1 can be charged by turning ON transistor S_2 to reduce the SC voltage ripple and improve the performance.

4) Output voltage = $\pm(V_{IN1} + V_{IN2})$ state: Capacitor C_2, charged to V_{IN1}, is connected in series with input voltage source V_{IN2} by turning ON transistors S_3 and S_4. Diodes D_1 and D_2 are reverse biased and hence block V_{IN1}. The net voltage that appears across the DC bus now is equal to $V_{IN1} + V_{IN2}$. Fig. 2(d) depicts the equivalent state for $V_0 = (V_{IN1} + V_{IN2})$. During this interval, capacitor C_1 can be charged by turning ON transistor S_2 to reduce the SC voltage ripple and improve the performance.

5) Output voltage = Zero level state: To obtain zero level at the output after the positive half cycle, only transistor Q_1 is turned ON, while all the other switches in the full bridge inverter remain turned OFF. The body diode of transistor Q_2, D_{Q2}, is employed for free-wheeling. Similarly, to obtain zero level at the output after the negative half cycle, only transistor Q_4 is turned ON, while all the other switches in the full bridge inverter remain turned OFF. In this case, the body diode of transistor Q_3, D_{Q3} is employed for free-wheeling. The switches in the front end DC level shifter remain in their previous states.

It is possible to charge the capacitor C_2 to $2V_{IN1}$ by turning ON transistors S_1 and S_5 to realize an output of V_{IN2}+2_{VIN1}. This will result in the output voltage steps becoming unequal. Let us consider this example when V_{IN1} = 20 V and V_{IN2} = 60 V. If $V_{C_2} = V_{IN1}$, then the output voltage steps would be $\pm$ 20V, $\pm$40V, $\pm$60V and $\pm$80V (Table I). If $V_{C_2} = 2V_{IN1}$,

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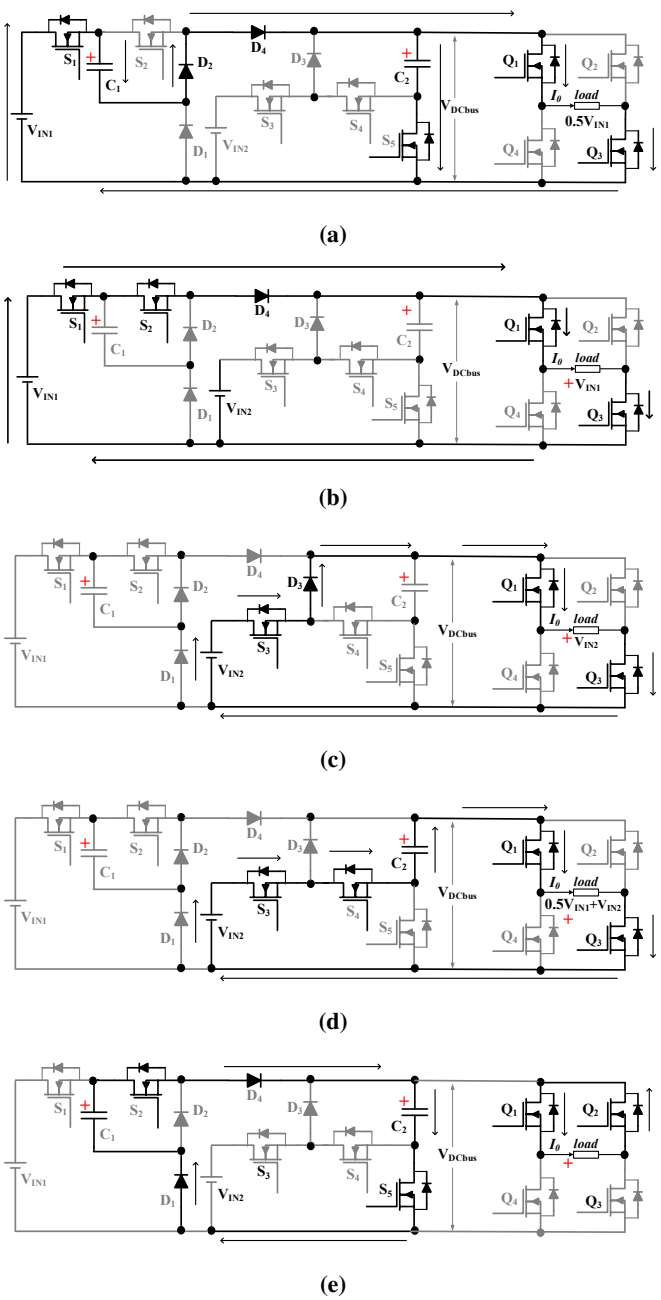

Fig. 3: Equivalent circuits of the proposed 9-level SC MLI to obtain different voltage levels (a) V_o = $0.5V_{IN1}$ (b) V_o = V_{IN1} (c) V_o = V_{IN2} (d) V_o = $0.5V_{IN1} + V_{IN2}$ (e) Zero state and balancing voltage of capacitor C_1 and C_2

then the output voltage steps would be ±20V, ±40V, ±60V and ±100V (Table I). If V_{C_2} = $2V_{IN1}$, the output voltage would have a higher step up ratio, however, the THD would be slightly poorer due to non-equal voltage steps as validated in section III of the paper.

B. Topology B description and operation principle

In the proposed SCMLI of Fig. 2, front end SC based DC-DC converter employs two input sources (V_{IN1} and V_{IN2}), five transistors (S_1, S_2, S_3, S_4 and S_5), four diodes (D_1, D_2, D_3 and D_4) and two capacitors (C_1 and C_2). DC levels obtained at the inverter DC bus include $0.5V_{IN1}$, V_{IN1}, V_{IN2}, $0.5V_{IN1} + V_{IN2}$. The H-bridge inverter employing transistors Q_1 to Q_4 effectively produces 8 bipolar levels ($\pm 0.5V_{IN1}$, $\pm V_{IN1}$, $\pm V_{IN2}$, $\pm(0.5V_{IN1} + V_{IN2})$) and a zero across the load. Table II explains the switching logic of the proposed inverter. The working states are explained in the following subsections.

1) Output voltage = $\pm 0.5V_{IN1}$ state: Capacitors C_1 and C_2, are charged to 50% the input voltage source V_{IN1} by turning ON transistors S_1 and S_5, through diodes D_2 and D_4. Transistors S_2, S_3, S_4 and diodes D_1 and D_3 remain turned OFF. The DC bus voltage at this state is equal to $0.5V_{IN1}$ as V_{IN2} is blocked by OFF transistor S_3. Fig. 3a depicts the equivalent state for $V_0 = +0.5V_{IN1}$.

2) Output voltage = $\pm V_{IN1}$ state: Transistors S_1 and S_2 are turned ON, which connects V_{IN1} to the DC bus through diode D_4. Transistors S_3, S_4 and S_5 remain turned OFF. Diodes D_1, D_2 and D_3 are reverse biased. Fig. 3b depicts the equivalent state for $V_0 = +V_{IN1}$.

3) Output voltage = $\pm V_{IN2}$ state: For normal operation of the proposed inverter, $V_{IN2} \neq V_{IN1}$. In the SC front end DC-DC converter, only transistor S_3 is turned ON while other transistors are turned OFF. Therefore, V_{IN2} is connected to the DC bus through diode D_3. Diodes D_1, D_2 and D_4 are reverse biased. Fig. 3c depicts the equivalent state for $V_0 = V_{IN2}$.

4) Output voltage = $\pm(0.5V_{IN1} + V_{IN2})$ state: Capacitor C_2, charged to $0.5V_{IN1}$, is connected in series with input voltage source V_{IN2} by turning ON transistors S_3 and S_4. All the diodes are reverse biased. The net voltage that appears across the DC bus now is equal to $0.5V_{IN1} + V_{IN2}$. Fig.3d depicts the equivalent state for $V_0 = (V_{IN1} + V_{IN2})$.

5) Output voltage = Zero voltage state: Under this state, the load is shorted to get a zero voltage across it by turning ON Q_1 and Q_3. In the front end side, this state is utilized to balance the capacitor voltages. The capacitor voltages are imbalanced since C_1 never discharges to the load. Therefore, by connecting C_1 and C_2 in parallel by turning ON S_2 and S_5, the capacitor voltages can be effectively balanced Fig.3e depicts the equivalent state for zero voltage state while balancing the capacitor voltages.

C. Topology improvisation

The proposed topologies can be further extended to increase the number of output voltage levels. A generalized front end topology for the proposed SCMLI in Fig.1a is shown in Fig.4a. An additional unit comprising of a voltage source and SC based double-mode circuit along with a few switches are included. If an additional voltage source V_{IN3} is added, then the output voltage levels would be $\pm V_{IN1}, \pm V_{IN2}, \pm V_{IN3}, \pm 2V_{IN1}, \pm 2V_{IN3}, \pm(V_{IN1} + V_{IN2}), \pm(V_{IN1} + V_{IN3}), \pm(V_{IN2} + V_{IN3}), \pm(2V_{IN2} + V_{IN3}), \pm(V_{IN1} + V_{IN2} + V_{IN3})$ and a zero level (21 bi-polar levels). Similarly, the same accentuated part can be added over the 21-level inverter to realize a higher level inverter. Switching logic for the generalized topology is given in Table III.

A generalized front end topology for the SCMLI proposed in Fig.1b is shown in Fig.4b. By inserting an additional voltage

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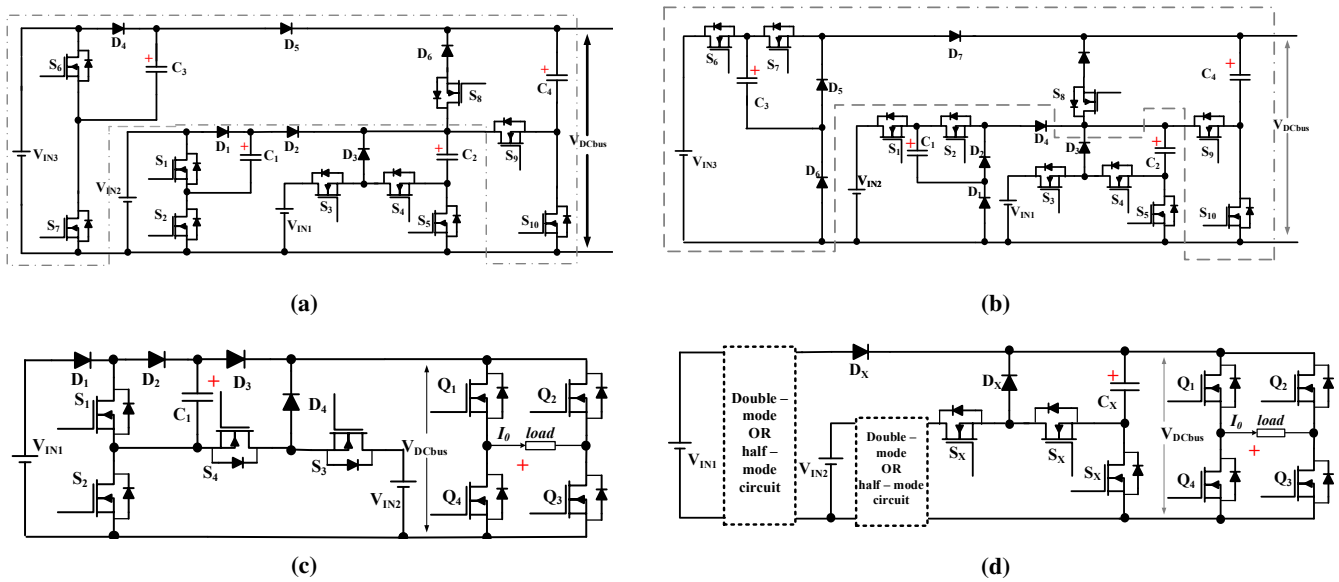

Fig. 4: (a) Generalized topology A with asymmetric sources. (b) Generalized topology B with asymmetric sources. (c) Modified topology A with fewer transistors and SCs. (d) General structure for SCMLI combining both half-mode and double mode SC converters.

TABLE III: Switching logic for the generalized topology for Fig. 1a

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_{DCBUS}
0	0	0	0	0	0	1	0	0	1	V_{IN3}
0	0	0	0	0	1	0	0	0	0	$2V_{IN3}$
0	1	0	0	1	0	0	1	0	0	V_{IN2}
1	0	0	0	0	0	0	1	0	0	$2V_{IN2}$
0	0	1	0	0	0	0	1	0	0	V_{IN1}
0	0	0	0	0	0	0	0	1	0	$V_{IN3} + V_{IN2}$
0	0	1	0	0	0	0	0	1	0	$V_{IN3} + V_{IN1}$
0	0	1	1	0	0	0	1	0	0	$V_{IN2} + V_{IN1}$
1	0	0	0	0	0	0	0	1	0	$2V_{IN2} + V_{IN3}$
0	0	1	1	0	0	0	0	1	0	$V_{IN1} + V_{IN2} + V_{IN3}$

source as shown, the new set of output voltages would be $\pm V_{IN1}, \pm V_{IN2}, \pm V_{IN3}, \pm 0.5V_{IN3}, \pm 0.5V_{IN2}, \pm(0.5V_{IN3} + 0.5V_{IN2}), \pm(V_{IN2}+0.5V_{IN3}), \pm(V_{IN1}+0.5V_{IN2}), \pm(V_{IN1}+ 0.5V_{IN3}), \pm(V_{IN1} + 0.5V_{IN2} + 0.5V_{IN3})$ and a zero level. Switching logic for the generalized topology is given in Table IV. A single unit is highlighted with dotted lines.

In the proposed topology A, shown in Fig. 1a, it can be observed that the switches S_2 and S_5 have identical switching logic (highlighted in Table I). Additionally, the SCs C_1 and C_2 are charged to the same voltage V_{IN1}. This provides an opportunity to merge both the switches and utilize a single SC to realize a nine-level output. Fig. 4c presents a modified topology eliminating one transistor (S_5) and an SC from the original topology A without sacrificing the number of output voltage levels. This innovation results in the cutting down the cost and the size of the inverter.

Fig.4d depicts a generic way of increasing the number of output voltage levels by inserting an SC double-mode or a half-mode circuit. Any one of the SC circuit can be cascaded to either of voltage sources to realize higher output voltage levels.

D. Comparisons with other proposed topologies

For the topology in Fig. 4a, the number of output levels are increased by inserting SC doubler circuitry to additional voltage sources whereas for topology in Fig. 4d, SC half circuitry is employed. Employing an SC doubler circuit increases the step-up capability of the SCMLI enabling relatively higher voltage operations thereby utilizing all the advantages of a lower current system. However, it also relatively increases the voltage stress of the H-bridge. Fig.4c shows an innovative way

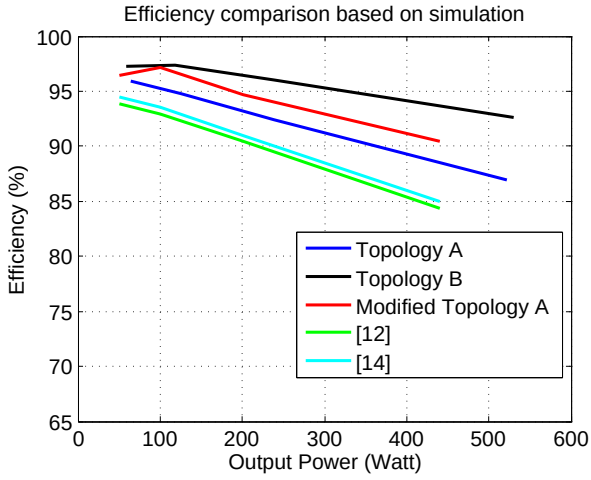

Fig. 5: Efficiency comparison of different topologies using simulation

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TABLE IV: Switching logic for the generalized topology for Fig. 1b

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_{DCBUS}
0	0	0	0	0	1	1	0	0	0	V_{IN3}
0	0	0	0	0	1	0	0	0	1	0.5 V_{IN3}
1	1	0	0	1	0	0	1	0	0	V_{IN2}
1	0	0	0	0	0	0	1	0	0	0.5 V_{IN2}
0	0	1	0	0	0	0	1	0	0	V_{IN1}
1	0	0	0	0	0	0	0	1	0	0.5 (V_{IN3}+ V_{IN2})
1	1	0	0	0	0	0	0	1	0	0.5 V_{IN3} + V_{IN2}
0	0	1	1	0	0	0	1	0	0	V_{IN1} + 0.5 V_{IN2}
1	0	0	0	0	0	0	0	1	0	V_{IN1} + 0.5 V_{IN3}
0	0	1	1	0	0	0	0	1	0	V_{IN1} + 0.5 V_{IN2} + 0.5 V_{IN3}

to reduce the active switches and SC count in the proposed inverter based on SC doubler (Fig.1a).

In Table V, several proposed SCMLI structures are compared with respect to the number of active switches (n_T) and diodes(n_D) used, number of output levels (n_l) generated and the number of voltage sources (i) by choosing the number of switched-capacitors employed (n) as the reference. It is seen that the proposed SCMLI offers a good trade-off between the number of components employed to the output levels generated. In Table VI, multi-input SCMLI topologies with symmetric output voltage levels are compared using cost function (CF), similar to the cost function analysis proposed in [17], [20]. The cost function is simplified and dependant only on the number of components. It is given by -

$$CF = \frac{(2n_T + n_D + n)n_{DC}}{n_l} \tag{1}$$

The cost function in the above equation takes into account the number of transistors and drivers, diodes, DC sources and SCs. For simplicity, the number of drivers is assumed to be equal to the number of transistors and written as $2n_T$. From Table VI, it can be seen that proposed family of SCMLI have a CF in the similar range with the Modified Topology A having the least CF. The topology from [20] and the Modified Topology A offer the least CF which means that they produce higher number of symmetric output voltage levels with fewer components.

Most SCMLI topologies in the literature, including the proposed family, employ fewer semiconductor switches and capacitors when compared to traditional MLI. The novel Fibonacci inverter proposed in Fig.2 of [25] uses fewer components than the conventional inverter. However, the proposed SCMLI employs relatively fewer components even when compared to the novel Fibonacci inverter. For example, to realize a 15-level inverter (7 x step up) the novel Fibonacci inverter employs eight SCs, twenty four transistors and six diodes with a single voltage source. In comparison, the proposed inverter can obtain twenty-one levels with only four SCs, fourteen transistors, six diodes and three asymmetric voltage sources.

The ability of the proposed family of inverters to drive large inductive loads is restricted. This limitation can be observed from the topology. This is because there is no path for the inductor current to flow to the ground during certain intervals. The maximum angle between the voltage and current can only be θ_1 (Refer Fig.6), similar to the topologies in [13], [24]. However, topologies proposed in [12], [17], [20] can drive large inductive loads. This is one shortcoming of the proposed family of SCMLI.

The efficiency comparison is carried out in Fig.5 for different nine level inverters under pure resistive loading. To obtain a fair comparison, the following parameters and non-idealities were chosen. $R_{dsON} = 0.09\Omega$, $R_{in} = 0.1\Omega$, $ESR = 0.05\Omega$, $R_d = 0.05\Omega$, $V_F = 0.42V$, $C = 1000\mu F$ and $f_S = 400Hz$. The peak voltage for all topologies was adjusted to $\pm$80 V with steps of $\pm$ 20 V. All the topologies were switched using staircase modulation. The common trend is that the efficiency drops as the power increases. Another observation is that with increase in the number of switches, and especially SCs, the fall in efficiency is higher. The proposed family of SCMLI utilizes the SC voltage only to obtain very few output voltage levels when compared to single source SCMLI proposed in [12], [13], [15], [17]–[19]. For example, topology A and B utilizes the SC voltage directly in four out of nine output voltage levels. The remainder levels are directly supported by the voltage source. In comparison, the topology proposed in [12], having the least efficiency among the compared ones, utilizes the SC voltage in five out of seven voltage levels. This allows the proposed family of SCMLI to operate at a comparatively higher efficiency as the loss effect from SC ripple voltage is mitigated.

III. Modulation strategies for the proposed SCMLI

Pulse width modulation (PWM) techniques for inverters can be broadly categorized into carrier based high frequency switching PWM and fundamental switching frequency based PWM. In high frequency switching PWM, the switching losses are severe as the transistors and diodes are commutated several times per switching cycle. In the case of fundamental switching frequency based PWM, the transistors are commutated just once or twice per switching cycle. This reduces switching loss considerably. However, high switching frequency techniques are popular as they can realize a better output voltage harmonic spectra. Since the HFAC inverters already switch at higher frequencies relatively to low-frequency switching inverter, fundamental switching frequency approaches are investigated to minimize the switching losses without compromising on the quality of the output voltage waveform quantified by the Total Harmonic Distortion (THD).

Staircase modulation is a subset of fundamental switching frequency which can further be classified into time and

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TABLE V: Comparison of SCMLI topologies

	n_T	n_D	i	n_l	Max voltage
Fig. 1 [12]	$3n+4$	0	1	$2n+3$	$(n+1)V_c$
Fig. 1 [13]	$n+5$	$2n$	1	$2n+3$	$(n+1)V_c$
Fig. 1 [14]	$6n$	n	n	$4n+1$	nV_{IN}
Fig. 2 [17]	$3n+3$	n	1	$2n+3$	$(n+1)V_c$
Fig. 3 [15]	$2n+4$	n	1	$2n+3$	$(n+1)V_c$
Fig. 2 [19]	$4n+1$	n	1	$4n+1$	nV_{IN}
Fig. 1 [20]	$4n+1$	$n/2$	$n/2$	$4n+1$	$4nV_{IN}$
Fig. 4 [24]	$3n+4$	$2n$	$n+1$	$2^{(n+2)}-1$	$\sum V_{ci}$+V_{IN_0}
Fig.4a	$2.5n+4$	$1.5n$	$(n/2)+1$	$6n-3$	$\sum V_{INi}$
Fig.4b	$2.5n+4$	$4n-4$	$(n/2)+1$	$6n-3$	$V_{IN1}+\sum V_{INi}/2$

TABLE VI: Comparison of SCMLI topologies with symmetric output voltage levels

	n_T	n_D	n	n_{DC}	n_l	CF
Topology A	9	3	2	2	9	5.11
Topology B	9	4	2	2	9	5.33
Modified Topology A	8	4	1	2	9	4.66
Fig. 8 [18]	10	1	1	3	13	5.07
[14]	12	2	2	2	9	6.22
[20]	18	2	4	2	18	4.66
[24]	10	4	2	3	15	5.2

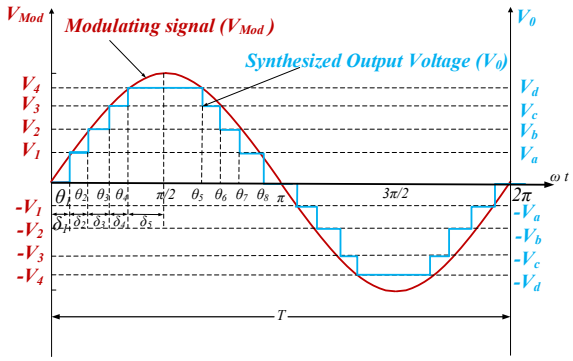

Fig. 6: Multilevel staircase modulation principle

frequency domain based approaches [18]. Simple staircase modulation employed for the proposed SCMLI is shown in Fig. 6. V_a, V_b , V_c and V_d are different output voltage levels corresponding to the value set by reference voltage levels V_1, V_2, V_3 and V_4 respectively. The reference voltages can either be set using potentiometers in analog controllers or the corresponding angles (θ_1, θ_2, θ_3 and θ_4) can directly be programmed into digital controllers. In this paper, two modulation approaches for the proposed inverters are studied.

A. Selective Harmonic Elimination

Selective harmonic elimination [27] is a popular example for the frequency domain based approach. This technique obtains the required fundamental output voltage and also eliminates specific lower order harmonics by choosing pre-calculated switching angles for a given modulation index. The major drawback of this technique is the demand for higher processing power to solve a set of non-linear transcendental equations as shown for an m-level inverter in (2) [24].

$$\begin{cases} cos\theta_1 + ... + cos\theta_s = zM_I \\ cos3\theta_1 + ... + cos3\theta_s = 0 \\ cos5\theta_1 + ... + cos5\theta_s = 0 \\ cos7\theta_1 + ... + cos7\theta_s = 0 \\ ..... \end{cases} \tag{2}$$

where the switching angles ($\theta_1..\theta_s$) are

$$0 < \theta_1 < \theta_2 < ... < \theta_s < \frac{\pi}{2} \tag{3}$$

where z $\left(z = \frac{m-1}{2}\right)$ is a function of the number of output levels. M_I is the modulation index (the ratio of the desired fundamental voltage (V_1) to the maximum obtainable fundamental voltage) given by (4)

$$M_I = \frac{\pi V_1}{4zV_{IN}} \tag{4}$$

For an m level inverter, $\left(\frac{m-1}{2}\right)$ specific harmonics can be eliminated as shown in (2). Triplen harmonics are usually not included in the SHE calculations as they cancel out themselves in a 3-phase inverter. Switching angles for various modulation indices (solutions for (2)) are plotted in Fig. 7. Fig. 7a and 7b shows the plot of the switching angles for a 7 level ($\theta_1, \theta_2, \theta_3$) and 9 level SCMLI ($\theta_1, \theta_2, \theta_3.\theta_4$) respectively, for a wide range of M_I. Fig. 7c shows the plot of THD versus M_I for both 7 level and 9 level SCMLI calculated using the corresponding switching angles. It is seen that the 9 level waveform has a lower THD value in comparison to the 7 level one. THD (γ) of the output waveform is given by (5). For three phase inverter output, triplen harmonics cancel out and therefore the THD is comparatively lower than their single phase counterparts.

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1} \tag{5}$$

B. Minimum THD

Nearest switching scheme [28] is a time domain based approach and demands relatively lesser processing power when compared to the SHE. Additionally, it is proven that this technique enables to obtain the minimum possible THD with equal and unequal input voltage sources [29], [30].

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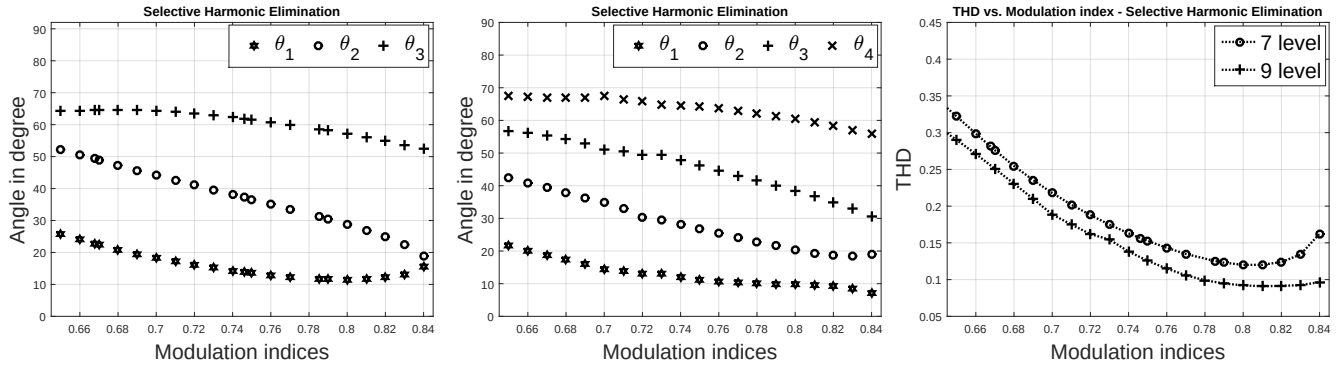

(a) **(b)** **(c)**

Fig. 7: Selective harmonic elimination angles for (a) 7 level inverter (b) 9 level inverter (c) THD vs modulation indices for 7 (with 5^{th} and 7^{th} harmonics eliminated) and 9 (with 5^{th}, 7^{th} and 11^{th} harmonics eliminated) level inverter

1) Equal voltage steps: A simple equation with a single variable for iteration to solve for the switching angles when the voltage steps are equal [29] is given by -

$$\sum_{i=1}^{s}\sqrt{1-\left(\frac{i-0.5}{s-0.5}\rho\right)^2}=sM_I \tag{6}$$

$$\theta_i = sin^{-1}\left(\frac{i-0.5}{s-0.5}\rho\right) \qquad i=1,2,...s. \tag{7}$$

where M_I denotes the modulation index, s denotes the number of number of H bridges in the given cascaded H-bridge inverter and ρ is the only variable to be solved. This technique is relatively simpler to implement on a digital control platform when compared to SHE because there is only one variable to be solved using iteration.

Fig.8a and Fig.8b shows the plot of different switching angles versus the modulation indices for seven-level and nine-level waveforms respectively. These angles are computed using (6) and (7). Fig.8c shows the plot of THD versus M_I for both seven-level and nine-level staircase waveform.

2) Unequal voltage steps: Similarly for staircase AC waveforms with unequal voltage steps, [30] provides a solution given by -

$$M_I=\sum_{k=1}^{s}e_k\sqrt{1-(\mu_k\rho)^2} \tag{8}$$

$$e_k=\frac{E_k}{\sum_{i=1}^{s}E_l} \tag{9}$$

$$\mu_k=\frac{\sum_{i=1}^{k}E_i-E_k/2}{\sum_{i=1}^{s}E_i-E_s/2} \tag{10}$$

$$\theta_k=sin^{-1}(\mu_k\rho) \qquad k=1,2..,s \tag{11}$$

In the above equations, E_k is the magnitude of the corresponding voltage step and E_s is the magnitude of the last voltage step (refer Fig. 2 in [30]). For the modulation scheme, the inputs to the algorithm include the magnitude of the voltage sources (E_1 to E_s) and M_I. The algorithm outputs switching angles ($\theta_1..\theta_s$) such that the THD of the output voltage waveform is minimum. Fig.8d and Fig.8e shows the plot of different switching angles versus the modulation indices for seven-level and nine-level waveforms respectively. These angles are computed using (8), (9), (10) and (11). Fig.8f shows the plot of THD versus M_I for both seven-level and nine-level staircase waveform when the voltage steps are unequal. For seven-level waveform the ratio of the unequal voltage sources were $E_1 : E_2 : E_3 = 10 : 8 : 17$. Similarly, for the nine-level waveform, the ratio of the unequal voltage sources were $E_1 : E_2 : E_3 : E_4 = 10 : 8 : 12 : 15$.

IV. Circuit Characteristics and Analysis

For the family of proposed multi-port SCMLI topologies, it is essential to identify the nature of the voltage sources that can be employed. There are several voltage sources available including batteries (Li-ion, Pb-acid, Ni based), super-capacitors and fuel cells. The type of voltage source to be employed can be analysed using the input current waveforms. Input current waveforms of both topology A and topology B are shown in Fig. 9a and Fig. 9b respectively. From these waveforms, it is clear that the input current of the voltage source V_{IN1} is relatively spiky and pulsating. Therefore, V_{IN1} can either be a super-capacitor bank or an old Pb-acid battery bank. The voltage source V_{IN2} which has a lesser spiky current profile can be a Li-ion battery. By choosing the voltage source keeping in mind the current profile, it is possible to extend the operating life of the energy source. Additionally, the waveforms also reveal vital information on the power requirements from each voltage source. HFAC SCMLI are used for a few kWs, like in an auxiliary power supply for a car or microgrids. The proposed multiport converters make an ideal choice as the aforementioned applications generally employ more than one type of voltage source.

In a SCMLI, the SC is charged by the input voltage source to a finite value and the energy stored in the SC is discharged to the load every cycle. During this cyclic process, there is a inherent loss due to several parasitic resistive components. They include the ESR, MOSFETs on-state resistances (R_{dsON}), voltage source internal resistances (R_{in}) and diode internal resistance (R_d). Therefore, the maximum voltage that the SC

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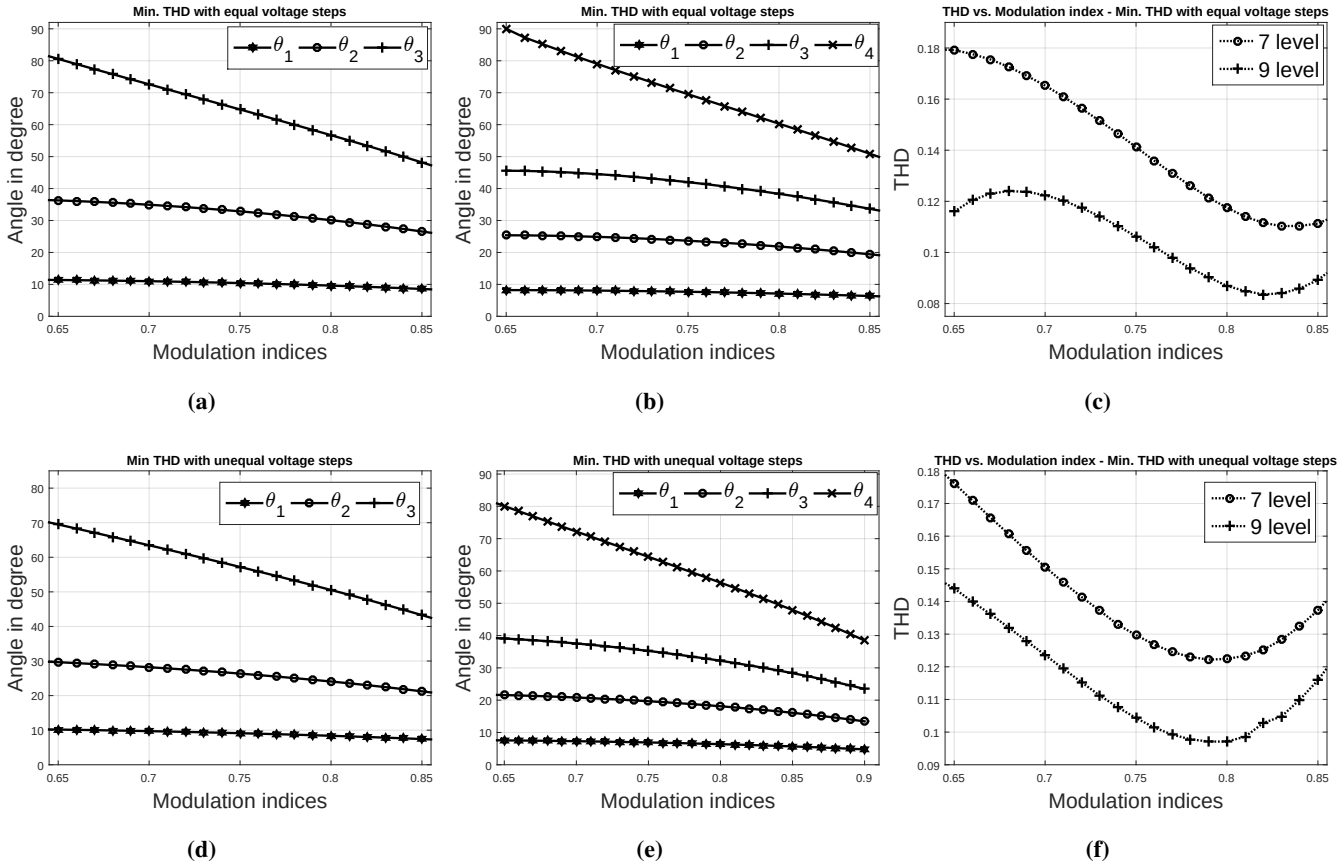

Fig. 8: Minimum THD angles with equal voltage steps for (a) 7 level inverter and (b) 9 level inverter. Minimum THD angles with unequal voltage steps for (d) 7 level inverter (ratio of sources were $E_1 : E_2 : E_3 = 10 : 8 : 17$) and (e) 9 level inverter($E_1 : E_2 : E_3 : E_4 = 10 : 8 : 12 : 15$). THD vs modulation indices for 7 and 9 level inverter for (c) equal voltage steps and (f) unequal voltage steps

TABLE VII: Least computed THD for different PWM switching schemes

PWM	SHE 7-level	SHE 9-level	MTHD eq 7-level	MTHD eq 9-level	MTHD uneq 7-level	MTHD uneq 9-level
M_I	0.8	0.81	0.83	0.82	0.79	0.8
THD	0.12	0.091	0.1103	0.0836	0.1222	0.0971

is charged to is determined by the net voltage drop across these resistive components and diode voltage drop (V_F), if any.

The general expression for RMS value of the m-level voltage staircase waveform (Fig. 6) is given by (12). If the SCMLI is connected to a R-L load then the I_{0RMS} is represented by (13)

$$V_{0_{RMS}} = \sqrt{\frac{2}{\pi}\left(V_a^2\delta_1 + V_b^2\delta_2 + ... + V_n^2\delta_n\right)} \qquad (12)$$

$$I_{0_{RMS}} = \frac{V_{0_{RMS}}}{\sqrt{(R_L)^2 + (X_L)^2}} \ \angle tan^{-1}\left(\frac{X_L}{R_L}\right) \qquad (13)$$

where, $V_a, V_b ... V_n$ are voltage levels at the output. For the nine-level SCMLI in Fig.1a, Fig.1b and Fig.4c the voltage levels are given by (14) (15) and (16) respectively.

$$\begin{cases} V_a = V_{IN1} - 2V_F - I_0(2R_{ds_{ON}} + R_{in}) \\ V_b = V_{IN1} + V_{C1} - V_F - I_o(3R_{ds_{ON}} + ESR + R_{in}) \\ V_c = V_{IN2} - V_F + I_o(3R_{ds_{ON}} + R_{in}) \\ V_d = V_{IN2} + V_{C2} - I_0(4R_{ds_{ON}} + R_{in} + ESR) \\ V_{C1} = V_{C2} \approx V_{IN_1} - V_F - I_{c1}(R_{ds_{ON}} + R_{in} + ESR) \end{cases} \qquad (14)$$

$$\begin{cases} V_a = V_{IN1} - V_{C1} - 2V_F - I_0(3R_{ds_{ON}} + R_{in} + ESR) \\ V_b = V_{IN1} - V_F - I_o(4R_{ds_{ON}} + R_{in}) \\ V_c = V_{IN2} - V_F + I_o(3R_{ds_{ON}} + R_{in}) \\ V_d = V_{IN2} + V_{C2} - I_0(4R_{ds_{ON}} + R_{in} + ESR) \\ V_{C1} = V_{C2} \approx 0.5V_{IN1} - I_C(2R_{ds_{ON}} + R_{in} + 2ESR) \end{cases} \qquad (15)$$

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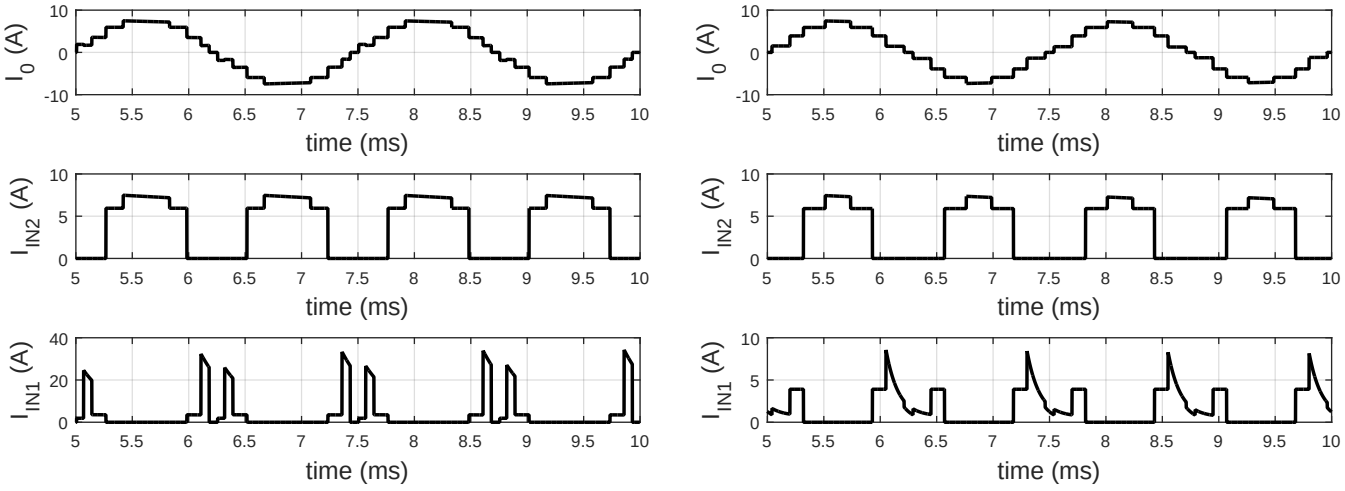

Fig. 9: Input currents (a) (I_{IN1} and I_{IN2}) profile for Topology A of Fig.1a and (b) (I_{IN1} and I_{IN2}) profile for Topology B of Fig.1b operating at 400 Hz

$$\begin{cases} V_a = V_{IN1} - 3V_F - I_0(2R_{ds_{ON}} + R_{in}) \\ V_b = V_{IN1} + V_{C1} - 2V_F - I_o(3R_{ds_{ON}} + R_{in} + ESR) \\ V_c = V_{IN2} - V_F + I_o(3R_{ds_{ON}} + R_{in}) \\ V_d = V_{IN2} + V_{C2} - I_0(4R_{ds_{ON}} + R_{in} + ESR) \\ V_{C1} \approx V_{IN1} - I_C(R_{ds_{ON}} + R_{in} + ESR) \end{cases} \tag{16}$$

A. Ripple analysis

The ripple voltage in general depends on the load current, fundamental frequency, and the value of the capacitance. For topology A (Fig.1a), the capacitors C_1 and C_2 are charged to a finite value (14) when connected in parallel to the input voltage sources. The capacitor C_1 and C_2 are discharged only during δ_3 (during $V_0 = 2V_{IN1}$) and δ_5 (during $V_0 = V_{IN1} + V_{IN2}$) respectively. This period occurs twice in a half cycle. Similarly in topology B (Fig.1b), C_1 and C_2 are charged to a finite value (14) and are discharged only during δ_3 and δ_5 respectively. The discharging period results in the voltage ripple across the SC which can be generically represented as –

$$\Delta V_C = \frac{\Delta Q_C}{C} = \frac{1}{\omega_S C}\int_{t_{d1}}^{t_{d2}} i_O sin(\omega_S t - \phi) d\omega_S t \tag{17}$$

where, t_{d1} and t_{d2} correspond to the net discharging period, ΔV_C is the voltage ripple, ΔQ_C is the amount of charge released during the period, i_0 is the output current with an angular frequency of ω_S lagging the output voltage by an angle ϕ. For the output waveform with equal voltage steps (the difference in the magnitude of succeeding output voltage steps are identical) scenario discharging to a purely resistive load (R_L), ΔQ_C can be further approximated to [13] –

$$\Delta Q_C i \approx \frac{V_0(2\delta_i)}{2\pi f_S R_L} \tag{18}$$

where, V_{IN} is the equal voltage step, R_L is the resistance of the load and f_S is the fundamental frequency of the output waveform. Therefore, the capacitors C_1 and C_2, in both topology A and B, can be computed using –

$$C_1 \geq \frac{2V_{IN1}\delta_3}{\pi f_S R_L \Delta V_{C1}} \tag{19}$$

$$C_2 \geq \frac{(V_{IN1} + V_{IN2})\delta_5}{\pi f_S R_L \Delta V_{C2}} \tag{20}$$

For the modified nine-level topology in Fig.4c, the solitary capacitor C_1 discharges during δ_3 (during $V_0 = 2V_{IN1}$) and δ_5 (during $V_0 = V_{IN1} + V_{IN2}$). Since the output current is larger during δ_5, the minimum capacitance for the modified topology (Fig.4c) can be computed by –

$$C_1 \geq \frac{(V_{IN1} + V_{IN2})\delta_5}{\pi f_S R_L \Delta V_{C1}} \tag{21}$$

B. Loss analysis

The loss in the SCMLI is the sum of transistor switching losses, conduction losses and switched-capacitor losses. The MOSFET switching losses is due to the losses incurred in cyclic charging and discharging of the MOSFET output capacitance C_T at transitor switching frequency (f_T). During the MOSFET turn-OFF transition, a linear increase in the drain-to-source voltage is observed. Therefore, C_T is charged from nearly zero volt to close to the input voltage V_T (equal to the voltage stress across the switch) . The power loss due to this phenomenon is given by [31] -

$$P_{sw} = V_T^2 C_T f_T \tag{22}$$

The above equation is true for a linear capacitance. Half of the total switching loss is dissipated in the MOSFET and the other in the charging path of the output capacitance C_T. For example, the net switching loss incurred by topology

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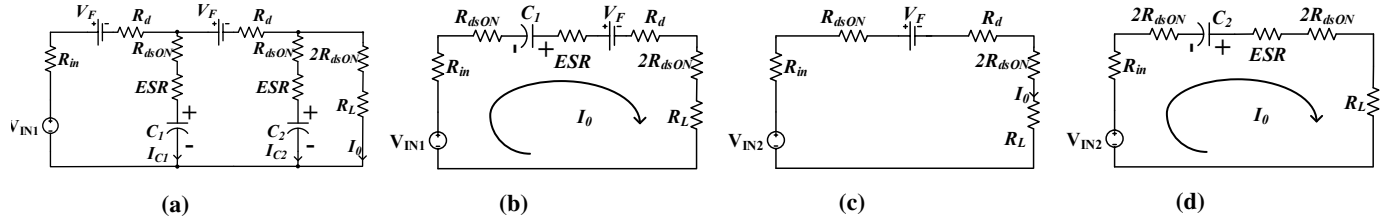

Fig. 10: Equivalent circuits of the nine-level SCMLI topology A during (a) Capacitors C_1 and C_2 charging, V_{IN1} level(b) Capacitors C_1 discharging, $2V_{IN1}$ level (c) V_{IN2} level (d) Capacitors C_2 discharging, V_{IN1} + V_{IN2} level

TABLE VIII: Conduction loss computation using output current

Output V.	V_{IN1}	$2V_{IN1}$	V_{IN2}	$V_{IN1}+V_{IN2}$
I_0	$\frac{V_{IN1}-2V_F}{R_{in}+2R_d+2R_{dsON}+R_L}$	$\frac{2V_{IN1}-V_F}{R_{in}+R_d+3R_{dsON}+R_L}$	$\frac{V_{IN2}-V_F}{R_{in}+R_d+3R_{dsON}+R_L}$	$\frac{V_{IN2}}{R_{in}+4R_{dsON}+R_L}$

A is presented. For the high bridge MOSFETs (Q_1 to Q_4), the maximum voltage stress for the topology A is equal to $V_{IN1}+V_{IN2}$. Similarly, for MOSFETs S_1 and S_2 the maximum voltage stress is V_{IN1}. For S_3, S_4 and S_5 the maximum voltage stress is V_{IN2}, (V_{IN2} - V_{IN1}) and $\sum V_{INi}$ respectively. The net maximum switching loss of topology A can be elaborated to -

$$P_{sw}=f_S(V_{IN1}+V_{IN2})^2\sum_{i=1}^{4}C_{Qi}+f_T\Big(2V_{IN1}^2C_{S1}+V_{IN2}^2 C_{S3}+(V_{IN2}-V_{IN1})^2C_{S4}+(V_{IN2}+V_{IN1})^2C_{S5}\Big). \tag{23}$$

where, C_{Sx} and C_{Qi} are output capacitances of the front end and H-bridge MOSFETs respectively and f_S is the fundamental frequency of the output. Switching loss in diodes ($P_{sw(D)}$) [32] is given by

$$P_{sw(D)}=\frac{V_D I_{rrp} f_s t_r}{6} \tag{24}$$

where, t_r is the time taken by the reverse recovery current to fall from its peak value of I_{rrp} to zero when a voltage of V_D is applied across the diode.

Conduction losses in the transistors and the diodes are due to their respective on-state resistances ($R_{ds_{ON}}$ and R_d). Similarly, conduction losses in the SC is due to their respective ESR. From Fig.10a, the maximum charging currents for the switched-capacitors C_1 and C_2 can be given by -

$$\begin{cases} I_{C1_{ch(m)}}=\dfrac{V_{IN1}-V_F-V_{C1i}}{R_{in}+R_d+R_{dsON}+ESR}=\dfrac{V_{eq1}}{R_{eq1}} \\ I_{C2_{ch(m)}}=\dfrac{V_{IN1}-2V_F-V_{C2i}}{R_{in}+2R_d+R_{dsON}+ESR}=\dfrac{V_{eq2}}{R_{eq2}} \end{cases} \tag{25}$$

The charging current $I_{Ci_{chRMS}}$ is given by

$$I_{Ci_{chRMS}}=\sqrt{\frac{2}{T}\int_{t_{ch1}}^{t_{ch2}}\left(I_{C_{(i)_{ch(m)}}}e^{-t/R_{eq(i)}C_{(i)}}\right)^2(t)dt} \tag{26}$$

where, T is the fundamental period, $t_{ch2}-t_{ch1}$ is the charging interval during which the peak capacitor charging current ($I_{C_{ch(i)(m)}}$) decays exponentially while being damped by the equivalent charging path resistance ($R_{eq(i)}$).

The SC discharging current $I_{Ci_{disRMS}}$ for C_1 and C_2 is equal to the magnitude of the output current during δ_3 and δ_5 respectively. The discharging current ($I_{C_{dis(i)}}$) (refer to Fig.10b and Fig.10d) trajectory is given by -

$$I_{C_{dis(i)}}=\frac{V_{dis_i}}{R_{eqd(i)}}\left(e^{-t/R_{eqd(i)}C_{(i)}}\right) \tag{27}$$

where, $R_{eqd(i)}$ is the equivalent resistance in the discharging path of the respective capacitors and V_{dis_i} is the initial value of capacitor voltage prior to their respective discharging periods. $I_{Ci_{disRMS}}$ is given by -

$$I_{Ci_{disRMS}}=\sqrt{\frac{2}{T}\int_{t_{dis1}}^{t_{dis2}}\frac{V_{dis_i}}{R_{eqd(i)}}\left(e^{-t/R_{eqd(i)}C_{(i)}}\right)^2} \tag{28}$$

where, the discharging period $t_{dis2}-t_{dis1}$ for SCs C_1 and C_2 is equal to the period during δ_3 and δ_5 respectively.

For conduction loss in the switches, it is assumed that the voltage levels V_1, V_2 etc (referring to Fig.6) are constant and do not change in the respective time intervals δ_1, δ_2 etc. The RMS current through different semiconductor switches can be computed from Table VIII and the capacitor current expressions computed above. Table VIII gives the expression for I_0 during different voltage levels. For example, the conduction loss in MOSFET S_2 and S_5 can be computed using the charging current of capacitor C_1 ($I_{C1_{chRMS}}$) and C_2 ($I_{C2_{chRMS}}$) respectively. Similarly, conduction loss of MOSFET S_1, S_3 and S_4 are computed using the RMS current of I_0 during $\pm 2V_{IN1}$ state, $\pm V_{IN2}$ and $\pm V_{IN1}+V_{IN2}$ states, and $\pm V_{IN1}+V_{IN2}$ state respectively. Conduction losses of diodes D_1, D_2 and D_3 are computed using RMS currents during the interval of $\pm V_{IN1}$, $\pm 2V_{IN1}$ and $\pm V_{IN2}$ respectively.

Assuming all transistors have equal $R_{ds_{ON}}$, all diodes have equal R_d, and all SC have equal ESR, the conduction losses in the circuit can be computed by -

$$\begin{cases} P_{con(T)}=\sum_{i=1}^{n_T} I_{T_iRMS}^2 R_{ds_{ON}} \\ P_{con(D)}=\sum_{i=1}^{n_D} I_{D_iRMS}^2 R_d \\ P_{con(SCdis)}=I_{C_{disRMS}}^2 ESR \\ P_{con(SCch)}=I_{C_{chRMS}}^2 ESR \end{cases} \tag{29}$$

The above set of equations suggests to employ switches and switched-capacitors with low internal resistances to mitigate

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TABLE IX: Simulation and Experimental parameters

V_{IN1} (V)	V_{IN2} (V)	min. C_1 and C_2 (F)	ESR (Ω)	R_{dsON} (Ω)	V_F (V)	R_L (Ω)	min. f_S (Hz)
20	60	560 μ	50 m	9 m	0.4	20	400

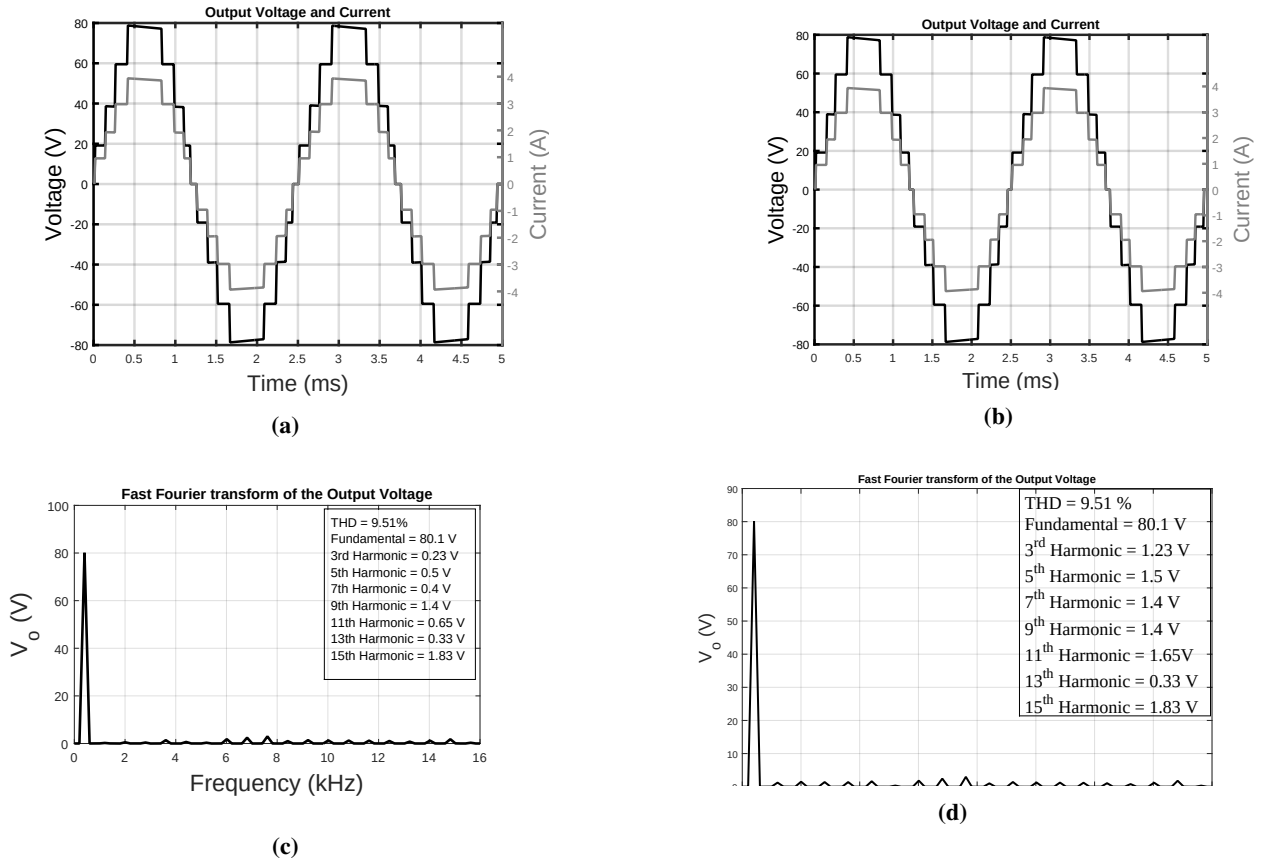

Fig. 11: Simulation results operating at M_I = 0.8 and fundamental frequency f_S = 400 Hz (a) Output voltage and current under SHE (b) Output voltage and current under Min. THD technique operating with equal voltage steps (c) FFT of the output voltage under SHE (d) FFT of the output voltage under Min. THD technique operating with equal voltage steps

conduction losses. Larger capacitance can be chosen to reduce the loss due to the capacitor ripple.

V. Results

The parameters are listed in Table IX. Simulation results, for the proposed topology A, depicting the output voltage and current waveforms and SC voltage and current waveforms are shown in Fig. 11. The simulation is carried out at M_I = 0.8 for both SHE and minimum THD with equal steps. The FFT waveforms for SHE and minimum THD with equal steps are depicted in Fig. 11c and Fig. 11d respectively. Under SHE, the 5^{th} and 7^{th} harmonic are minimized to 0.5 V and 0.4 V respectively. The harmonics are not equal to zero since non-ideal components are employed during simulations. Additionally, the switching angles have decimal points and are difficult to emulate during simulations. For minimum THD with equal steps the THD is relatively lower than that under SHE. This confirms the theoretical evaluation and plots in and Fig. 7c and Fig. 8c.

Experiment verification for topology A is carried out with the same parameters. The voltage and current waveforms of the output and the SC operating at 400 Hz are shown in Fig. 12. Fig. 13 show the waveforms at different output power frequency and power levels. At higher power levels, the voltage droop in the output waveform is higher due to higher voltage ripple (plotted in Fig. 17b). However, the ripple proportionately reduces with increase in the output frequency for a given value of capacitance as explained in (17).

FFT of the output voltage for SHE modulation is shown in Fig. 14a. The digital oscilloscope displays the RMS value of the amplitude of different frequency components. The 5^{th}, 7^{th} and 11^{th} harmonic are minimized (around 1 V) similar to the simulation results. FFT results for minimum THD modulation is shown in Fig. 14b. The 3^{rd}, 5^{th} and 7^{th} harmonics are comparatively larger when compared to the SHE modulation scheme, similar to theoretical and simulation observations. FFT results under minimum THD scheme with unequal voltage steps (Fig. 14c) show higher value of lower order harmonics in comparison.

The proposed SCMLI topology A is tested with different R-L loads and the waveforms are shown in Fig. 15. Fig.15a and 15b depict 400 Hz waveforms of output voltage and current

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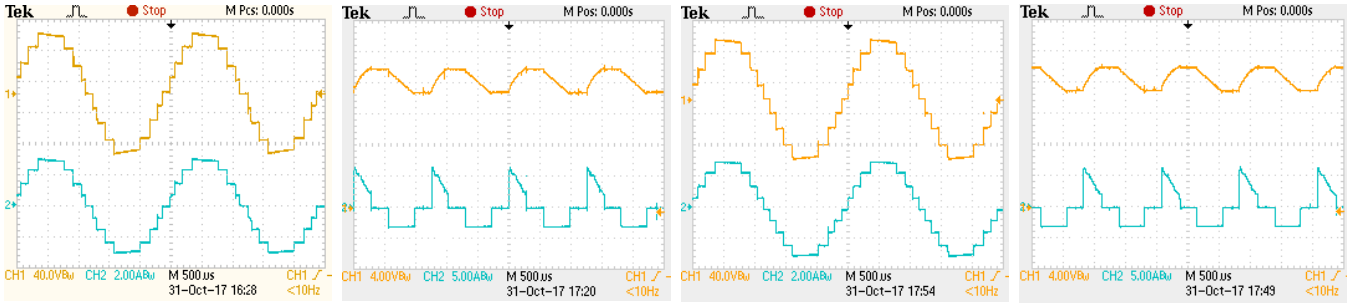
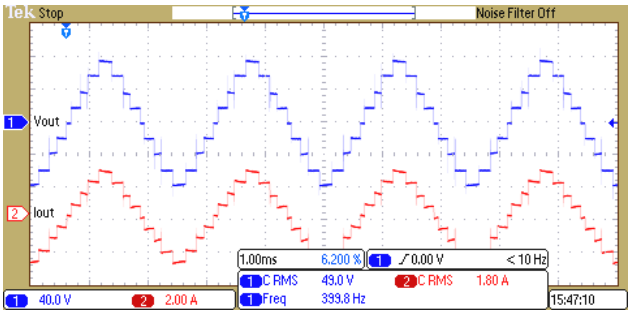
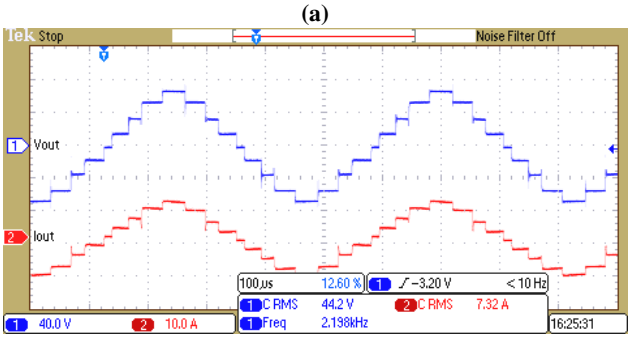


(a) **(b)** **(c)** **(d)**

Fig. 12: Experimental results operating at f_S = 400 Hz. (Ch.1 - Voltage, Ch.2 - Current) (a) Output voltage and current under SHE (M_I = 0.8) (b) switched capacitor voltage and current under SHE (d) Output voltage and current under Min. THD technique operating with equal voltage steps (M_I = 0.82) (e) switched capacitor voltage and current under Min. THD technique operating with equal voltage steps



(a)



(b)

Fig. 13: Experimental results (a) Output voltage and current at 400 Hz with output power of 88 W (b) Output voltage and current at 2200 Hz with output power of 320 W [23]

driving a 25 Ω-220 μH and 16.7 Ω-220 μH load respectively. Fig.15c and 15d depict 400 Hz waveforms of output voltage and current driving a 25 Ω-440 μH and 16.7 Ω-440 μH load respectively. It can be observed that the current waveforms driving the 440 μH load is more sinusoidal. The ability of the proposed SCMLI to drive loads with larger inductance value is limited as discussed in section II D.

The dynamic loading experiment is performed on topology A and the results are shown in Fig.16. In Fig.16a and 16b, initially the SCMLI is driving a pure 25 Ω load. Another pure 50 Ω is added in parallel using a switch to increase the load current by approximately 50%. Similarly, in Fig.16c and 16d, initially the SCMLI is driving a pure 16.7 Ω (25 Ω in parallel with 50 Ω) load. The 50 Ω is removed from the current path by opening the switch to lower the load current by 33%. It is seen that under both scenarios the SCMLI responds well.

Fig. 17a shows the measured plot of efficiency versus output power at different output frequencies. Fig. 17b shows the measured plot of capacitor (C_2) peak to peak ripple versus output power at different frequencies. With increase in frequency, the peak to peak capacitor voltage reduces. This in turn reduces the conduction loss in the capacitor and contributes to higher efficiency. The efficiency drops with increase in output power. This can be mitigated by employing larger switched-capacitors, designing zero voltage switching or zero current switching front end converters and by choosing transistors with low R_{dsON}, diodes with low V_f.

VI. Conclusions

This article proposes a family of SCMLI topologies for high frequency AC applications. The asymmetric sources employed have a common ground enabling simpler design. Inherent charging of the capacitors every half-cycle solves the problem of capacitor voltage imbalance afflicting conventional MLI. Operating principles of the two topologies proposed are discussed in detail with suggestions for improvements. Generalized topology structure is derived and compared to several existing topologies. Table V shows that the proposed SCMLI offers a good trade-off with respect to the number of components employed to generate a specific number of voltage levels. Such inverters are extremely beneficial at situations where several DC sources are available, for example in the case of renewable energy farms. To achieve higher power, it is better to employ multiple DC sources as input to a single inverter than connecting several individual DC sources fed inverters in parallel.

Two different staircase modulation approaches - frequency-domain based selective harmonic elimination and time-domain based minimum THD schemes were investigated. Minimum THD scheme can even be used when the output voltage waveform steps are not equal. Several switching angle versus modulation indices plots for three variations of the aforementioned staircase modulation approaches are presented. These plots give an idea to the reader on how the switching angles typically vary with modulation index. THD values for the corresponding switching angles are computed and plotted against modulation indices to obtain better understanding of the variation of THD with modulation index and the region of

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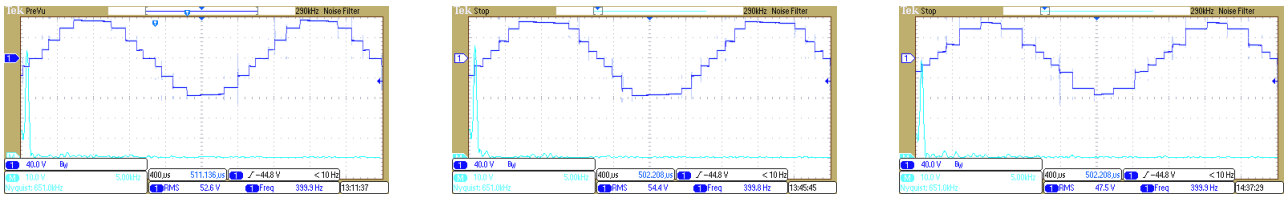
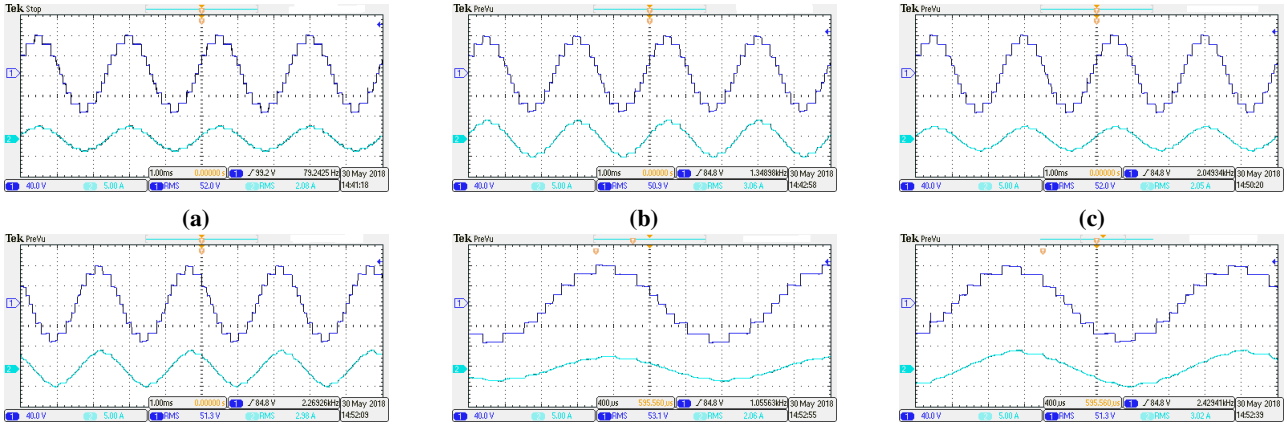


(a) **(b)** **(c)**

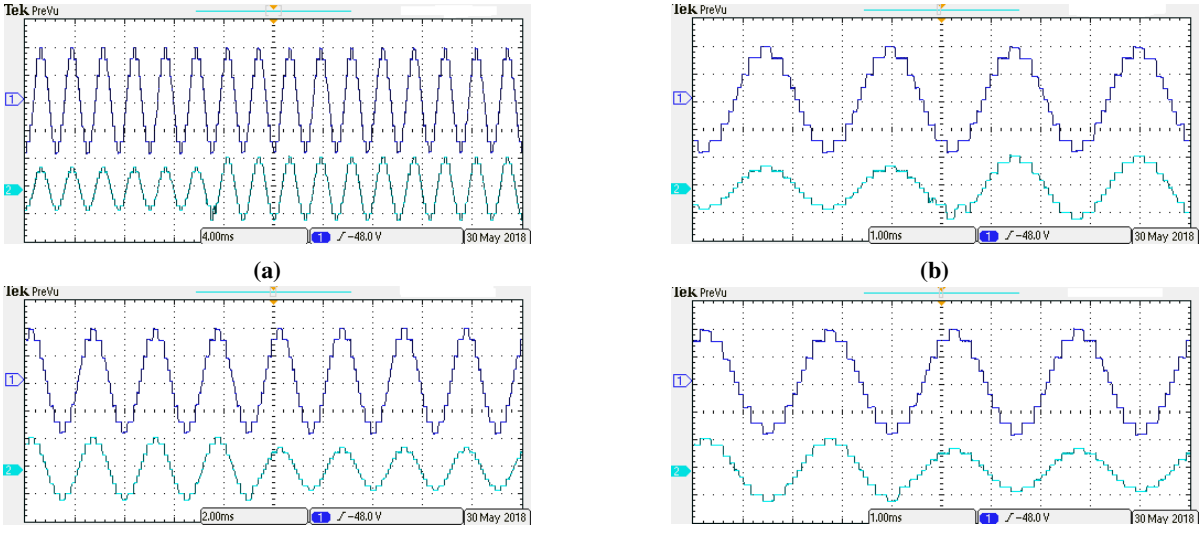
Fig. 14: Experimental results (a) FFT of the output voltage under SHE technique operating (b) FFT of the output voltage under Min. THD technique operating with equal voltage steps (c) FFT of the output voltage under Min. THD technique operating with unequal voltage steps (Step size = 15V, 15V, 30V, 15V)



(a) **(b)** **(c)**

(d) **(e)** **(f)**

Fig. 15: Experimental results with R-L load (a) 25 Ω, 220 μH (b) 16.7 Ω, 220 μH (c) 25 Ω, 440 μH (d) 16.7 Ω, 440 μH (e) Zoomed in waveform 25 Ω, 220 μH (f) Zoomed in waveform 16.7 Ω, 440 μH. Channel 1 - Output voltage, scale - 40 V per division. Channel 2 - Output current, scale - 5 A per division.



(a) **(b)**

(c) **(d)**

Fig. 16: Experimental results with dynamic loading (a) and (b) 50% increase in load current (c) and (d) 33% decrease in load current. Channel 1 - Output voltage, scale - 40 V per division. Channel 2 - Output current, scale - 5 A per division

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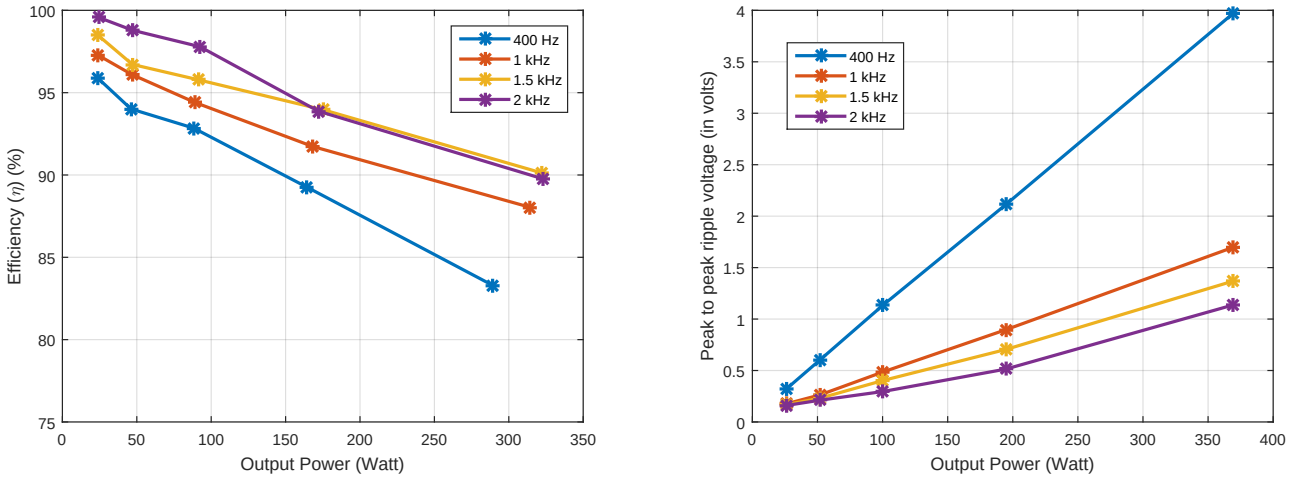

(a) **(b)**

Fig. 17: Measured at M_I = 0.8 using SHE for Topology A (a) efficiency versus output power at different output frequencies (b) peak to peak capacitor ripple voltage (V_{C2}, C_2 = 560μF) versus output power at different output frequencies

the plot at which the THD is minimum. The proposed topology A is tested under both modulation schemes. The experimental results validate the theoretical and simulation outcomes.

ACKNOWLEDGMENT

This work was supported by Innovation and Technology Fund and the Automotive Parts and Accessory Systems R&D centre under Project GHP/057/14AP. The authors wish to acknowledge the support provided by the members of the Power Electronics Research Centre (PERC) at The Hong Kong Polytechnic University. The authors appreciate the reviewers and the associate editor for their valuable suggestions which helped improve the quality of the paper.

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